

REMARKS

Claims 1-20 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion. New claims 21 through 26 have been added.

I. The Prior Art Rejections

Claims 1-2, and 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Temple, et al. (U.S. Patent No. 5,654,226), hereinafter referred to as Temple. Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Delgado, et al. (U.S. Patent No. 5,091,331), hereinafter referred to as Delgado, in view of Yoshihara, et al. (U.S. Patent No. 6,555,901), hereinafter referred to as Yoshihara. Applicants respectfully traverse these rejections based on the following discussion.

A. Rejections of Claims 1-7 Under 35 U.S.C. §103(a) Based on Temple.

The Applicants respectfully traverse the rejection of independent claim 1 based on Temple because Temple does not teach or suggest the following patentable features: (1) "providing a supporting wafer comprising oxide regions in a substrate and having a planar surface at which said oxide regions and said substrate are exposed"; and (2) "partially joining an integrated circuit wafer to said planar surface ... such that ... said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent" method steps.

Temple teaches a method of processing wafers in which a device wafer 10 is selectively bonded to a carrier wafer 12 (see column 2, line 62 – column 3, line 2). Figures 2A-F illustrate exemplary bonds 18 that are formed between the carrier wafer 12 and the device wafer 10. These bond structures 18 are located on the wafer surfaces, not within the wafers, such that spaces are also formed between the two wafers (see Figures 2A-F and column 3, lines 11-55). Only the bonds 18 connect wafers 11 and 12. The surfaces of the wafers 10, 12 do not contact each other. Thus, carrier wafer 12 does not

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physically support the device wafer 10 other than at the bonding sites 18. Those skilled in the art will recognize that the lack of physical support across the entire surface of the device wafer can result in warpage during high temperature processes as well as cracking or other damage during thinning or cutting processes.

Contrarily, the present invention first provides a supporting wafer that comprises oxide regions in a substrate and has a planar surface at which these oxide regions and the substrate are exposed (see paragraphs [0035-0037] and Figure 7). This supporting wafer can be formed by performing a patterned etch process through a nitride layer and oxide layer into a substrate 12 (see Figure 5). Then, an oxide region 40 is formed in the etched portions of the substrate 12 (see Figure 6) and the wafer is planarized such that it includes regions of oxide 40 along the smooth upper surface of the substrate 12. Thus, the supporting wafer is configured to adequately support the integrated circuit wafer so as to avoid warping and cracking during subsequent processing.

After the support wafer is formed, an integrated circuit wafer is partially joined "to said planar surface ... such that ... said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent" method steps (see paragraphs [0037-0039] and [0051] and Figures 8-10). Specifically, the integrated circuit wafer can be aligned above the support wafer (see paragraph [0037] and Figures 8-9). A thermal oxide bonding process joins the two wafers only at the joining points 88 (i.e., at the surface of the oxide regions) (see paragraph [0038]). The planar upper surface of the supporting wafer, including the oxide regions and the substrate, maintains contact with the integrated circuit wafer (see paragraph [0051] and Figure 9). Consequently, the upper surface, and not simply the bonds (as illustrated in Temple) maintains contact with and mechanically supports the integrated circuit wafer during subsequent processing and cutting so as to increase yield by reducing damage to devices (i.e., chip sections) that are formed from the integrated circuit wafer (see paragraph [0051] and Figures 9-14).

The Office Action acknowledges that Temple does not disclose oxide regions at the planar surface of the supporting wafer but supports the rejection of claim 1 based on

In re Karlson, 136 USPQ 184 ("omission of an element and its function in combination where the remaining elements perform the same function as before involves only routine skill in the art"). Specifically, the Office Action states that "any non-thermal bonding material may be used in filling the gaps without affecting the scope of the prior art teachings." The Applicants respectfully disagree because filling in the gaps of Temple with a non-thermal bond would eliminate the non-bonded areas between the integrated circuit wafer and the supporting and, thus, would eliminate a significant feature of the present invention (i.e., cutting through integrated circuit wafer would not form chip sections but rather would form sections of the integrated circuit wafer still bonded to the support wafer).

Furthermore, the Office Action provides that "the applicant has not disclosed planarizing the surface solves any stated problem, or is for any particular purpose, and the invention appears to perform equally well with prior art teachings". This essentially amounts to a utility rejection under 35 U.S.C. §101 and §112. MPEP§2107 provides that "any rejection based on lack of utility should include a detailed explanation why the claimed invention has no specific and substantial credible utility." This section of the MPEP further provides that "a *prima facie* showing must establish that it is more likely than not that a person of ordinary skill in the art would not consider that any utility asserted by the applicant would be specific and substantial."

The Applicants respectfully submit that a *prima facie* showing of lack of utility has not been met. Specifically, the Applicants submit that the supporting wafer of the present invention as configured with oxide regions at the planar surface has a specific and substantial utility and that this utility is supported in the specification and would be recognized by one skilled in the art. Specifically, paragraph [0051] discloses that the supporting wafer maintains contact with and supports the integrated circuit wafer during processing and cutting so as to increase yield by reducing damage to chips that are formed from the integrated circuit wafer (see paragraph [0051 and Figures 9-14). The Applicants also assert herein and in the previously filed Amendment under 37 C.F.R. 1.111 that those skilled in the art will recognize that avoiding the spaces between the two

wafers that are disclosed in Temple (i.e., by forming the supporting wafer with the oxide regions at the planar surface and not with bonding structures above the surface of the supporting wafer) increases the mechanical strength of the bonded supporting wafer/device wafer structure in order to avoid wafer warpage during subsequent high temperature processes as well as to reduce chip damage during thinning and cutting processes. Additionally, those skilled in the art will recognize that by maintaining contact with the integrated circuit wafer, the support wafer can also be used to dissipate heat from the integrated circuit wafer.

Therefore, amended independent claim 1, is patentable over Temple. Furthermore, dependent claims 2-7 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that claims 1-7 are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection of Claims 1-20 Under 35 U.S.C. §103(a) Based on Delgado.

The Applicants respectfully traverse the rejection of independent claims 1, 8 and 15 based on Delgado because Delgado does not teach or suggest the following patentable features: (1) "providing a supporting wafer comprising oxide regions in a substrate and having a planar surface at which said oxide regions and said substrate are exposed"; and (2) "partially joining an integrated circuit wafer to said planar surface ... such that ... said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent" method steps (e.g., processing, thinning, and/or cutting).

Delgado teaches a method of fabricating a wafer that incorporates bonding a pair of wafers together in order to perform wafer thinning and formation steps on one of the wafers and, particularly, a method for dicing thin wafers (see column 1, lines 7-10 and lines). Specifically, as described in column 3, lines 10-19, a wafer 10 is formed such that

it has a surface with oxidized peaks 22 and valley regions 24. A handle wafer 30 is also formed such that it has a planar bonding surface 32 with an oxide bonding layer 40 covering the entire bonding surface. The two wafers 10 and 30 are pressed together and heated such that only the peaks 22 of wafer 10 bond with the surface of wafer 30.

Alternatively, the surface of the handle wafer has the peaks and valleys (see column 3, lines 53-58). Thus, as with Temple (discussed above) in the Delgado invention spaces exist between the wafers (see Figure 1C, Figure 1D, Figure 5A, Figure 5B, Figure 6, and Figure 7) and the wafer 10 is only physically supported by the peaks 22 (i.e., the bonding structure) and not the handle wafer 30 itself. Those skilled in the art will recognize that the lack of physical support across the entire surface of the device wafer can result in wafer warpage due to subsequent high temperature processes as well as cracking or other damage during thinning or cutting processes.

As mentioned above, the present invention first provides a supporting wafer that comprises oxide regions in a substrate and has a planar surface at which these oxide regions and the substrate are exposed (see paragraphs [0035-0037] and Figure 7). After the support wafer is formed, an integrated circuit wafer is partially joined "to said planar surface ... such that ... said substrate does not bond with but maintains contact with said integrated circuit wafer so as to support said integrated circuit wafer during subsequent" method steps (see paragraphs [0037-0039] and [0051] and Figures 8-10). Since the support wafer surface is planar and no peaks or valleys are formed on the surface of either the integrated circuit wafer or the supporting wafer (as illustrated in Delgado), the two wafers abut each other (see Figure 10). Thus, the planar upper surface of the supporting wafer, including the oxide regions and the substrate, maintains contact with the integrated circuit wafer (see paragraph [0051] and Figure 9). Consequently, the upper surface, and not simply the bonds (as illustrated in Delgado) maintains contact with and mechanically supports the integrated circuit wafer during subsequent processing and cutting so as to increase yield by reducing damage to devices (i.e., chip sections) that are formed from the integrated circuit wafer (see paragraph [0051] and Figures 9-14).

As with regard to the rejections of claims 1-7 based on Temple, the Office Action

acknowledges that Delgado does not disclose oxide regions at the planar surface of the supporting wafer and supports the rejection of claims 1, 8, and 15 based on *In re Karlson*, 136 USPQ 184. Specifically, the Office Action states that "any non-thermal bonding material may be used in filling the gaps without affecting the scope of the prior art teachings." The Applicants respectfully disagree because filling in the gaps of Delgado with a non-thermal bond would eliminate the non-bonded areas between the integrated circuit wafer and supporting wafer and, thus, would eliminate a significant feature of the invention (i.e., cutting through integrated circuit wafer would not form chip sections but rather would form sections of the integrated circuit wafer still bonded to the support wafer).

Furthermore, the Office Action provides that "the applicant has not disclosed planarizing the surface solves any stated problem, or is for any particular purpose, and the invention appears to perform equally well with prior art teachings". This essentially amounts to a utility rejection under 35 U.S.C. §101 and §112. MPEP§2107 provides that "any rejection based on lack of utility should include a detailed explanation why the claimed invention has no specific and substantial credible utility." This section of the MPEP further provides that "a *prima facie* showing must establish that it is more likely than not that a person of ordinary skill in the art would not consider that any utility asserted by the applicant would be specific and substantial."

The Applicants respectfully submit that a *prima facie* showing of lack of utility has not been met. Specifically, the Applicants submit that the supporting wafer of the present invention as configured with oxide regions at the planar surface has a specific and substantial utility and that this utility is supported in the specification and would be recognized by one skilled in the art. Specifically, paragraph [0051] discloses that the supporting wafer maintains contact with and supports the integrated circuit wafer during processing and cutting so as to increase yield by reducing damage to chips that are formed from the integrated circuit wafer (see paragraph [0051] and Figures 9-14). The Applicants also assert herein and in the previously filed Amendment under 37 C.F.R. 1.111 that those skilled in the art will recognize that avoiding the spaces between the two

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wafers that are disclosed in Delgado (i.e., by forming the supporting wafer with the oxide regions at the planar surface and not with peaks of oxide material above the surface of the supporting wafer) increases the mechanical strength of the supporting wafer/device wafer structure in order to avoid local wafer warpage during subsequent high temperature processes as well as to reduce chip damage during thinning and cutting processes. Additionally, those skilled in the art will recognize that by maintaining contact with the integrated circuit wafer, the support wafer can also be used to dissipate heat from the integrated circuit wafer.

Therefore, amended independent claims 1, 8 and 15 are patentable over Delgado. Further, dependent claims 2-7, 9-14 and 16-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that claims 1-20 are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

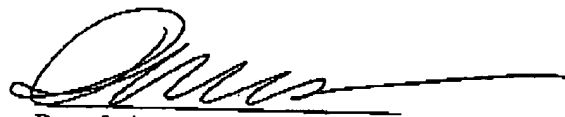
With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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